REMARKS

Claims 1-18 are pending. Claims 1-14 and 16 are rejected. Claim 17 is allowed and claim 15 is objected to. Claim 18 is subject to a restriction requirement. Applicants respectfully request reconsideration of the Application in view of the attached amendments and the remarks set forth below. By this communication, claims 19-29 have been added, and claim 18 has been cancelled. Claims 15 and 17 have been amended. In order to be allowable, claim 15 has been amended to include the claim limitations of independent claim 4.

RESTRICTION

The above reference Office Action recites a restriction requirement grouping claim 1-17 into Group I and claim 18 into Group II. Applicants respectfully traverse this restriction requirement because claims 1-17 and claim 18 are related to programmable logic. However, applicants elect Group I and cancel claim 18 to expedite prosecution of the current application.

REJECTIONS UNDER 35 U.S.C. § 102(e)

Claims 1-11, 13, 14, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,550,042 to Dave (hereinafter "Dave"). Applicants respectfully traverse these rejections.

Dave discloses a co-synthesis technique for generating a hardware and software architecture for a systems-on-a-chip from an input embedded system specification. Specifically, in support of this §102(e) rejection, the Office Action relies on col. 3, lines 1-30, which recites that the embedded systems-on-a-chip comprises one or more general

processor cores, RAMs, ROMs, programmable logic blocks, functional macros based on standard cells, analog buffers, etc.

Claim 1 of the present application recites the steps of identifying a programmable logic core and integrating the programmable logic core into the designed application specific circuit. As depicted in FIG. 1 of Dave, Dave teaches a SOC with general processor cores and programmable logic blocks but does not teach the programmable processor core as recited in claim 1. The Office Action does not specify whether the general processor cores or the programmable logic blocks of Dave anticipate the programmable logic core as recited in claim 1. In either case, both the general processor cores and the programmable logic blocks of Dave do not anticipate the programmable logic core. A closer reading of Dave reveals that the general processor cores are "off-the shelf" (col. 3, line 11), "general-purpose" processor cores (col. 3, lines 17-18). Therefore, the general processor cores of Dave are not programmable to the extent of not being able to reconfigure the processor core as can be performed by a programmable logic core. The programmable logic blocks of Dave are not cores as specified by programmable logic cores in claim 1. Furthermore, Dave does not teach or anticipate the step of *identifying* the programmable logic core and *integrating* the programmable logic core into the designed application specific circuit.

Additionally, claim 1 also recites the steps of identifying an application and designing an application specific circuit for the application. The Examiner relies on col. 1, lines 61-67 for a teaching of an Application Specific Integrated Circuit (ASIC) application. While this section of Dave does mention an ASIC, this section does not teach ASIC applications as suggested by the Examiner. In contrast, claim 1 recites two separate elements of an application and an application specific circuit, which are recited in the step of designing an

application specific circuit for the application. Dave does not teach or suggest these two separate elements of an application and an application specific circuit as recited in claim 1. Therefore, claim 1 is allowable over Dave for at least the above stated reasons.

In regards to claim 2, the same argument that Dave does not anticipate "programmable logic cores" also applies to claim 2. Therefore, Dave does not teach or suggest the steps of establishing a set of timing constraints associated with the programmable logic core and controlling the design of application specific circuitry that interfaces with the programmable logic core in the integrated circuit. Therefore, claim 2 is allowable over Dave for at least the above stated reasons.

In regards to claims 3-4, the same argument that Dave does not anticipate "programmable logic cores" also applies to claims 3-4. Furthermore, the Office Action fails to state how Dave teaches the limitation of a "sign-off design." Nevertheless, Dave does not mention a sign-off design for satisfying timing constraints. Therefore, claims 3-4 are allowable over Dave for at least the above stated reasons.

Claim 5 is allowable for at least the same reasons as claim 4 is allowable over Dave. Additionally, Dave does not teach or suggest all the claim limitations of claim 5. In support of this rejection for claim 5, the Examiner relies on col. 3, lines 10-30 to teach the application circuit interface and the programmable logic adapter. Dave in col. 3, lines 10-30 teaches interconnections and interfaces between modules of the hardware architecture of the embedded systems-on-a-chip. However, this teaching is too high-level and vague to teach with any specificity the limitations of an application circuit interface for providing a signal interface between the programmable multi-scale array and the application specific circuitry as recited in claim 5. Also, the interconnections and interfaces of Dave clearly do not teach or

suggest a programmable logic core adapter that configures the programmable multi-scale array as recited in claim 5. Therefore, claim 5 is allowable over Dave for at least the above reasons.

Claims 6-11, 13, and 14 are allowable for at least the same reasons as claim 5. Additionally, applicant traverses the assertion that the claim limitations of claims 6-11, 13 and 14 are well known and request the Examiner to provide documentation that these claim limitations are well known.

In regards to claim 16, the same argument in claim 1 that Dave does not anticipate "programmable logic cores" also applies to claim 16. Therefore, Dave does not teach or suggest means for performing functions associated with a programmable logic core. Additionally, the Office Action fails to state how Dave teaches the limitation of a "sign-off design." As stated before, Dave does not mention a sign-off design. Therefore, claim 16 is allowable over Dave for at least the above stated reasons.

REJECTION UNDER 35 U.S.C. § 103(a)

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dave in view of U.S. Pat. No. 6,377,912 to Sample et al. (hereinafter "Sample"). Applicants respectfully traverse this rejection.

Claim 12 is allowable over Dave for at least the same reasons discussed above for claim 4 because claim 12 is dependent on claim 4. Additionally, neither Dave, Sample nor the combination of Dave and Sample teach or suggest all the claim limitations of claim 12. Claim 12 recites configuration data control logic, scan path logic, and application circuit interface logic. The section of Dave that the Examiner relies on for this rejection, which is

col. 3, lines 10-30, does not mention the configuration data control logic. Once again, the cited portion of Dave only teaches interconnection, interfaces, and synthesis at a high-level without going into the specific teaching of configuration data control logic as recited in claim 12.

Sample discloses a hardware emulation system that time multiplexes multiple design signals onto physical logic chips on a printed circuit board. Sample discloses scan chains in col. 4, lines 1-12 but does not teach scan path logic. Therefore, claim 12 is allowable over Dave and Sample for at least the above stated reasons.

CONCLUSION

Therefore, in view of the above remarks this application is in condition for allowance, and the Examiner is respectfully requested to allow this application. The Examiner is invited to contact Applicants' undersigned representative regarding any issues that the Examiner feels are still outstanding.

Respectfully submitted,

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